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A DISTRIBUTED AMPLIFIER USING TRANSISTORS

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APRIL 28, 1961

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CALIFORNIA INSTITUTE OF TECHNOLOGY

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Contents

Abstract

A distributed amplifier with a stable gain of 10, risetime of 2.5 nanoseconds for 125 ohm load impedance is described. The maximum output voltage is 3.2 volts with negative polarity. The amplifier consists of 2 stages of 6 Philco 2N1742 transistors each and an emitter follower using a 2N1500.

Design formulae are derived and detailed performance of a specific amplifier is given.

Acknowledgment

The valuable suggestions and comments of Matthew Sands are gratefully acknowledged.

I Introduction

During the period since the first distributed amplifier was constructed[1)], a wide variety of instruments have been built[2,6)]. The advent of transistors with gain-bandwidth products in the kilomegacycle region suggests the possibility of their use in high speed distributed amplifiers.

The longer lifetime of transistors (Table 1) makes the construction of complex, reliable equipment feasible. The smaller operating voltages of a transistor lead to less consumed power as an advantage and smaller available output voltage as a disadvantage. The high intrinsic mutual conductance provides a possibility for strong emitter degeneration resulting in stable gain, while the relatively small input impedance causes losses in the input delay line which, in most cases, amount to several per cent. The high frequency performance of today's transistors is considerably limited by their relatively high collector to base capacitance, which also results in more involved computations.

II Equivalent Circuit

The hybrid equivalent circuit of Fig. 1 has been used as the basis of the subsequent calculations. Although it is accurate only for times longer than τ_o, [3,4,5)] it has been found to provide a reasonably good (25 per cent) approximation for times comparable to τ_o.

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1) Ginzton, "Distributed Amplification", PIRE 36 (1948).
2) Lewis and Wells, "Millimicrosecond Pulse Techniques", McGraw-Hill (1954).
3) Barna, Marshall, Sands, A Nanosecond Coincidence Circuit using Transistors, Nuclear Instruments and Methods 7 (1960).
4) Middlebrook, "Introduction to Junction Transistor Theory", Wiley and Sons (1957).
5) Barna, Some Transistor Small Signal Equivalent Circuit Calculations, Calif. Inst. of Tech. Synchrotron Lab. Report CTSL-22.
6) Tektronix, Type 581 Oscilloscope Manual.

TABLE 1.

Comparison of Typical High-Frequency Transistor and Tube Parameters*

Parameter	Transistor	Pentode
Lifetime	10^6 hours	10^4 hours
Power dissipation	50mW	5W
Output voltage	5V	100V
Mutual conductance	200mA/V	20mA/V
Input impedance	10^3 ohms	10^7 ohms
Gain-bandwidth product	1 kMc	0.2 kMc
Transfer capacitance	1.0pF	0.01pF

*In grounded emitter and grounded cathode configurations.

The intrinsic time constant of the transistor, τ_o, is related to the gain-bandwidth product, f_o, by:

$$\tau_o = \frac{1}{2\pi f_o}$$

The Laplace transform of the current transfer can be written as:

$$L\left[\frac{is}{ie}\right] \cong \frac{\alpha}{1 + p\,\tau_o}$$

III Basic Configuration

The emitter degenerated base input configuration shown in Fig. 2 has been used. The choice of R_e determines the effective "g_m" and part of the input capacitance:

$$C_{in} = \frac{\tau_o}{R_e'} + C_{stray} + C_{Miller}$$

where $R_e' = R_e + r_e$. The value of the Miller capacitance is

$$\left(1 + \frac{R_L}{R_e'}\right)C_{cb} \equiv K\,C_{cb}$$

This input capacitance is paralleled by an input resistance of $\beta R_e'$.[5] The input impedance of the transistor constitutes the shunt element of a base delay line section (Fig. 3). In order to have a constant iterative impedance of Z_b, the series element of a delay line section has to be the dual network of the parallel element. This, approximating $r_s \ll Z_b/2$, $r_s \ll \beta R_e'$, requires a resistance of $Z_b/\beta R_e'$ in series with an inductance of Z_b^2/C_{in} as the series element. Taking the base spreading resistance into account as a correction, the 10 per cent to 90 per cent risetime of a section can be approximated by $T_{ri} \cong 1.1(Z_b + 2r_s)C_{in}$. The risetime of a line consisting of n sections is approximately:

$$T_{rs} \cong T_{ri}\, n^{1/3} \cong 1.1\,(Z_b + 2r_s)\, C_{in}\, n^{1/3}$$

For smooth transient response, proper mutual inductance is required between adjacent sections[7]. The attenuation per section for $r_s \ll \beta R_e'$ can be written as:[8]

$$\varepsilon \cong \frac{Z_b}{\beta R_e'}$$

and the average signal on n sections can be approximated by:

$$V_{ave} = V_{in} \exp\left(-\frac{\varepsilon n}{2}\right)$$

The collector impedance is mainly capacitive: $C_c = k\, C_{cb} + C_{stray\ coll.}$. If this is arranged to constitute a shunt element of a delay line (Fig. 3) with a velocity of propagation equal to that of the base line, the currents of the individual transistors will be added with the correct phase. This requires that $Z_b C_{in} = Z_c C_c$, where Z_c is the characteristic impedance of the collector delay line.

The voltage amplification of a stage of n transistors is:

$$M_v = \frac{\alpha Z_c}{2 R_e'}\, n \exp\left(-\frac{\varepsilon n}{2}\right)$$

If Z_c is not equal to Z_b, the power gain (M_p) is more significant and for an output load of Z_c it can be written as

$$M_p^{1/2} = M_s = \frac{\alpha Z_c}{2 R_e'} \left(\frac{Z_b}{Z_c}\right)^{1/2} n \exp\left(-\frac{\varepsilon n}{2}\right) = M_i\, n \exp\left(-\frac{\varepsilon n}{2}\right)$$

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7) Elmore and Sands, "Electronics: Experimental Techniques", McGraw-Hill (1949).

8) Reference data for radio engineers, IT/T (1956).

where

$$M_i = \frac{\alpha Z_c}{2 R_e'} \left(\frac{Z_b}{Z_c} \right)^{1/2}$$

IV Amplifier Consisting of M Stages

If M stages, consisting of n transistors each, are cascaded, the resulting gain can be written as:*

$$M_M = M_s^{\;M} = \left[M_i \; n \exp\left(- \frac{\varepsilon n}{2}\right) \right]^M$$

and the 10 per cent to 90 per cent risetime as

$$T_{rm} = T_{rs} \sqrt{M} = 1.1 \, (Z_b + 2r_s) \, C_{in} \, n^{1/3} \sqrt{M}$$

The gain bandwidth product of such an amplifier is:

$$(GB) \cong \frac{M_M}{\sqrt{2\pi} \, T_{rm}} = \frac{1}{\sqrt{2\pi}} \; \frac{\left[M_i \; n \exp\left(- \frac{\varepsilon n}{2}\right) \right]^M}{1.1 \, (Z_b + 2r_s) \, C_{in} \, n^{1/3} \sqrt{M}}$$

To determine the optimum configuration for a total number of $N_o = nM$ transistors, we use the following approximations:

$$r_s \ll Z_b/2$$

$$\tau_o = \text{const.}$$

$$Z_b = \text{const.}$$

$$Z_c = \text{const.}$$

$$M_i = \text{const.}$$

$$\alpha \cong 1$$

$$C_{stray} \approx 0$$

---

* If $Z_b \neq Z_c$, the relationships are valid if an impedance matching transformer is inserted between adjacent stages.

If we express C_{in} by means of M_i, Z_c, Z_b, N_o, n and take

$$\frac{\partial}{\partial n} \ln (GB) = 0$$

this will provide the optimum gain-bandwidth product for a given number of transistors. The solution gives $M_s = nM_i = \exp (1 + 1/6M)$. For a large number of stages $(M \gg 1/6)$, we can write:

$$M_s \cong e \cong 2.71$$

V Risetime of a Stage with an Amplification of e, as a Function of Transistor Parameters

If we assume that the optimum stage gain of e = 2.71 is chosen, and restrict ourselves to $Z_b = Z_c = Z$, and approximate $r_s \ll Z/2$, $\alpha \cong 1$, $C_{stray} \cong 0$, the risetime of a stage can be written as:

$$T_{rs} = 2.2 \, \tau_o \, e \, n^{-2/3} \left[1 + (1 + \frac{n}{e}) \frac{Z}{2} \frac{C_{cb}}{\tau_o} \right] .$$

T_r/τ_o is plotted in Fig. 4 as a function of ZC_{cb}/τ_o with n as a parameter.

Figure 5 provides a set of graphs of risetimes for Z = 50 ohms and Z = 125 ohms and different values of n as a function of τ_o with C_{cb} as a parameter. The approximate values of τ_o and C_{cb} of the transistors of Fig. 5 are the following:

Type	Typ. τ_o(ns)	Typ. C_{cb}(pF)	Symbol
2N502A	0.4	1.5	o
2N769	0.25	2	□
2N1141	0.35	1.8	Δ
2N1500	0.3	2.5	◗
2N1742	0.2	1.5	⊗

VI Application of Emitter Followers

Emitter followers may be applied as isolation stages between collector lines and subsequent loads. By their use, one doubles the maximum output voltage, but restricts the polarity to negative for PNP transistors.

For $r_e \ll R_L$, the risetime of an emitter follower is approximately $2.2\ \tau_o$,[5)] the input capacitance is $\tau_o/R_L + C_{cb}$ and the input resistance is $\beta\, R_L$; R_L being the load resistance. For a source resistance of R_s, the output impedance is

$$r_e + \frac{R_s + r_s}{\beta}$$

If an emitter follower is used to separate equal source and load impedances, it provides a "gain" of almost 2 with a risetime of $\approx 2.2\ \tau_o$. Thus there is an optimum number of emitter followers for a given gain and risetime. The computation of this optimum leads to involved algebra and has not been completed.

VII Analysis of an Amplifier with an Amplification of 10, Risetime of 2.5 Nanoseconds (Fig. 6)

Approximate values of the transistor parameters are the following:

2N1742	τ_o	$\cong$ 0.2 ns
	C_{cb}	$\cong$ 1.5 pF
	r_s	$\cong$ 8 ohms
2N1500	τ_o	$\cong$ 0.3 ns
	C_{cb}	$\cong$ 2.5 pF
	r_s	$\cong$ 5 ohms

Both types were selected to have a minimum beta of 50.

The transistors are operated at a DC current of 4 mA (see Fig. 6), thus $r_e = KT/q\,I \cong 6.3$ ohms, $R_e' = R_e + r_e = 121 + 6.3 = 127.3$ ohms. The input impedance of the amplifier was required to be 125 ohms. For $n = 6$ and $Z_c = 100$ ohms, the input capacitance of a section can be approximated as:

$$C_{in} \cong \frac{\tau_o}{R_e'} + \left(1 + \frac{Z_c}{2\,R_e'}\right) C_{cb} + C_{stray}$$

$$= \frac{0.2 \text{ ns}}{127.3 \text{ ohms}} + 1 + \frac{100}{2\text{x}127.3} \; 1.5 \text{ pF} + 1 \text{ pF} = 4.65 \text{ pF}$$

The rise time of a stage

$$T_{rs} \cong 1.1\,(Z_b + 2r_s)\,C_{in}\,n^{1/3} = 1.1(125{+}2\text{x}8)4.65 \text{ x } 6^{1/3} = 1.32 \text{ ns}$$

The delay per section (T_d)

$$T_d \cong Z_b\,C_{in} = 125 \text{ ohms x } 4.65 \text{ pF} = 580 \text{ ps}$$

which has to be equal to the delay of a collector line section:

$$Z_c\,C_c = 580 \text{ ps}$$

The capacitance of the collector line is composed of the following parts:

Miller capacitance:	$c_b \left(1 + \frac{Z_c}{2\,R_e'}\right) = 2.1$ pF
Collector to case capacity in series with case to ground capacitor:	1.2 pF
Collector to emitter capacity:	1.0 pF
Stray capacity:	1.5 pF

These total to 5.8 pF. This results in a collector line impedance of 100 ohms. The inductance per section of the delay lines is:

$$L_b = 2T_d\ Z_b = 125 \text{ ohms } 580 \text{ ps} = 72.5 \text{ nH}$$

$$L_c = 2T_d\ Z_c = 100 \text{ ohms } 580 \text{ ps} = 58 \text{ nH}$$

The collector line terminating voltage resistors were chosen unequal (82.5 and 124 ohms) with a geometric mean of 100 ohms in order to obtain a higher output voltage. The effects of the reflections tend to cancel and no significant change in the transient response of the amplifier was observed as a consequence of this.

The required series resistance in a base line section is given by:

$$R = \frac{Z_b^{\ 2}}{\beta R_e'} = \frac{125^2}{75 \times 127.3} = 1.65 \text{ ohms}$$

The attenuation per section by:

$$\varepsilon = \frac{Z_b}{\beta R_e'} = \frac{125}{50 \times 127.3} = 1.96 \times 10^{-2} = 1.96 \text{ per cent}$$

The amplification of the first stage can be written as:

$$M_1 = \frac{\alpha}{R_e'} \frac{Z_c Z_b}{Z_c + Z_b} n \exp\left(-\frac{\varepsilon n}{2}\right)$$

$$= \frac{0.98}{127.3} \frac{82.5 \times 125}{82.5 + 125} 6 \exp\left(-\frac{1.96}{100} \frac{6}{2}\right) = 2.15$$

The amplification of the second stage is higher, since the collector line is terminated only at one end:

$$M_2 = \frac{\alpha}{R_e'} Z_c\ n \exp\left(-\frac{\varepsilon n}{2}\right) = \frac{0.98}{127.3}\ 124 \times 6 \times 0.942 = 5.4$$

The gain of the emitter follower is:

$$M_{EF} = \frac{\beta R_L}{\beta R_L + Z_c + \beta r_e} = \frac{50 \times 115}{50 \times 115 + 124 + 50 \times 8} = 0.915$$

where $R_L = 115$ ohms is the load on the output terminals of the amplifier. The total amplification of the amplifier is:

$$M_{MN} = 2.15 \times 5.4 \times 0.915 = 10.6$$

The risetime of the emitter follower is approximately:

$$T_{re} \cong 2.2\ \tau_o\ \frac{Z_c + r_s}{R_L} = 2.2 \times 0.3 \times \frac{124 + 5}{115} = 0.74 \text{ ns}$$

The total risetime of the amplifier is computed as:

$$T_{rt} \cong \sqrt{2\ T_{rs}^{\ 2} + T_{re}^{\ 2}} = \sqrt{2 \times 1.32^2 + 0.74^2} \cong 2 \text{ ns}$$

The risetime was measured to be 2.5 nanoseconds. The total delay is:

$$T_{d,tot} = 2n\ T_d + \tau_o = 2 \times 6 \times 0.606 + 0.3 \cong 8 \text{ ns}$$

VIII Construction

The circuit has been built on a 4.5" x 8" epoxy glass printed circuit board (Fig. 7).

The base line consists of six sections of 3 turns of No. 34 copper wire and 5 turns of No. 40 Constantan resistance wire. The collector line consists of six sections of 5 turns of No. 28 copper wire. Both coils are encapsulated (Fig. 8).

The input and output connections are made via the printed circuit board connector and an 0.1 output monitor is provided at a coaxial connector mounted on the front. Special care has been taken in laying out the ground connections in order to avoid any ground loops.

Two shield plates are used, one on each side of the amplifier board to provide capacitive shielding from adjacent units.

IX Pulser Tests

The transient response of the amplifier has been tested using a sampling oscilloscope with resistive adapters to provide 125 ohm source and load impedances for the amplifier under test. Step and simulated photomultiplier pulses were used as inputs. The measurements were conducted with the output terminals of the input base line externally terminated by 125 ohms. At this point, the input signal is available with deteriorated risetime and amplitude for secondary use.

The results of the measurements with step pulse input are shown in Fig. 9, with typical pulse shapes shown in Figs. 10 to 13. In the case of simulated photomultiplier tube pulses (risetime of 3 ns, width of 12 ns), Figs. 14 and 15 show the slight deterioration of risetime and amplitude caused by the non-ideal response of the amplifier.

The gain as a function of the power supply voltages was measured, resulting in less than ± 1 per cent change of the gain for ± 5 per cent change in any of the power supply voltages.

X Performance

The amplifier was primarily designed for use with fast coincidence circuits at the Caltech 1.5 GeV Synchrotron. The small amplitude of pulses from photomultiplier tubes looking at Cerenkov and scintillation counters often requires amplification in order to provide the -2.3 volt pulse height required to drive the fast coincidence circuits.

At the present time, four similar circuits are being used in a counter telescope experiment for detecting K^+ mesons. Coincidence resolving times as short as 4 ns with pulse height variations as large as one to four have been achieved. The two circuits used with the Cerenkov counters successfully handled counting rates up to 20 Mc.

The output signal of the input base line has been integrated in the 50 ns time range and used for pulse height analysis. Since this signal is not effected by the saturation of the output stage, the amplifier can be operated in its saturated region without the loss of input pulse height information.

These amplifiers have been in continuous operation for over three months without any failure and have exhibited stable performance during this period. Presently, the addition of several amplifiers is planned as fast preamplifiers for stable amplification of small signals.

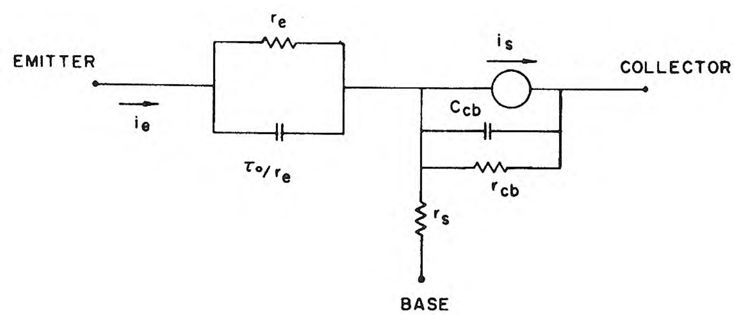


FIG. I <u>TRANSISTOR EQUIVALENT CIRCUIT</u>

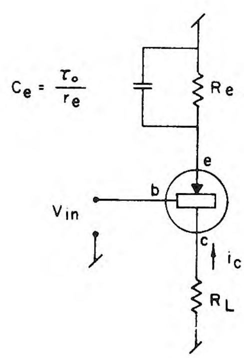


FIG. 2 <u>BASIC CONFIGURATION</u>

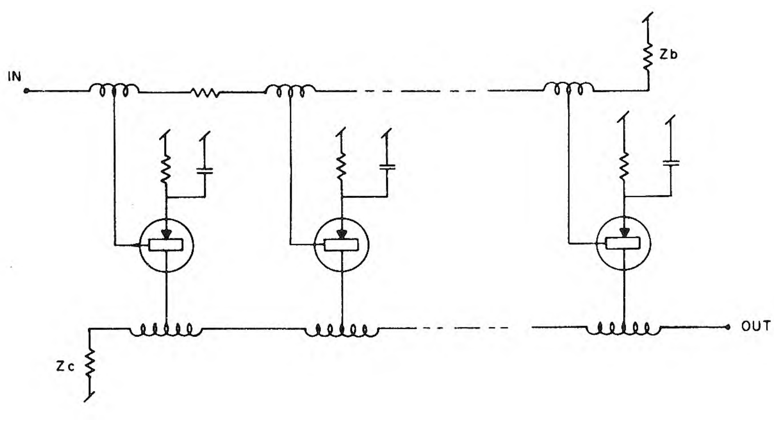


FIG. 3 BASIC CONFIGURATION OF A STAGE.

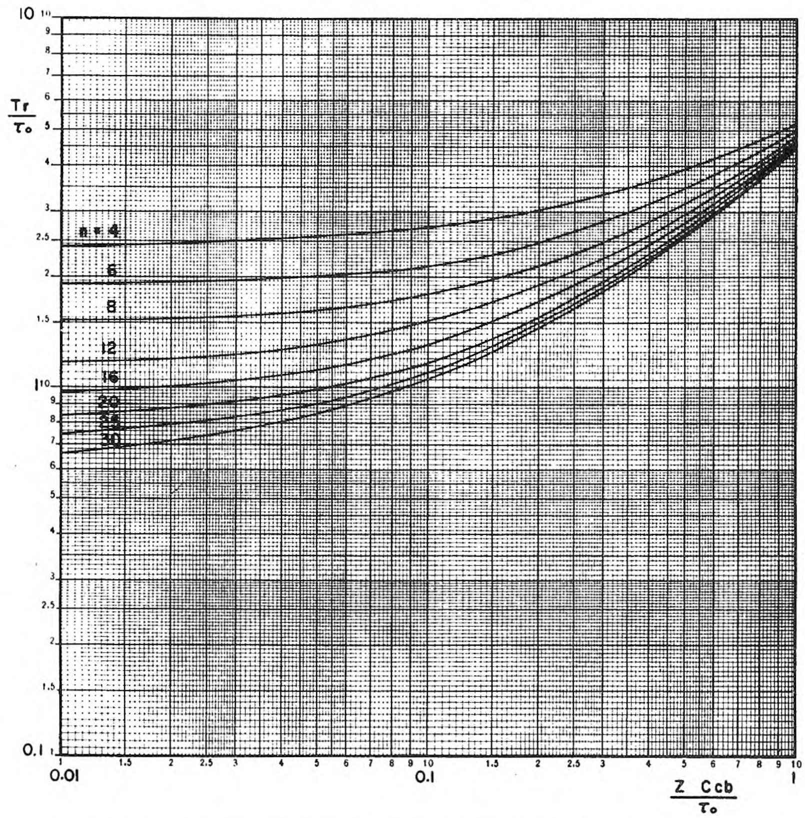


FIG. 4 RISETIME OF A STAGE WITH A GAIN OF e AS FUNCTION OF $\frac{Z\,C_{cb}}{\tau_o}$ WITH n AS PARAMETER.

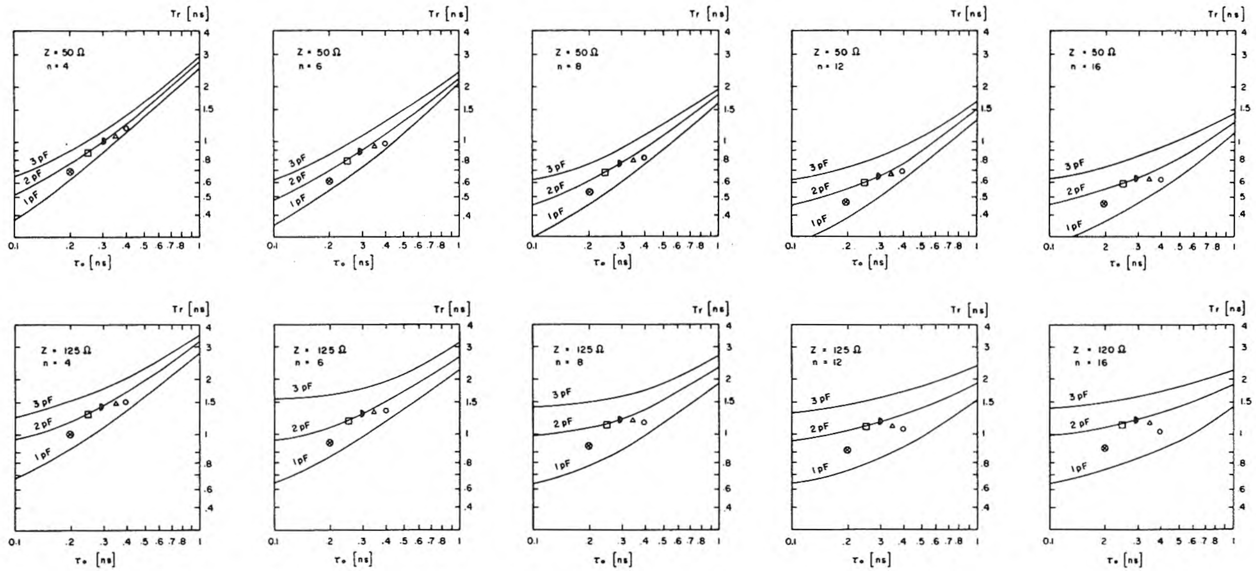


FIG. 5. RISETIME OF A STAGE WITH A GAIN OF e AS FUNCTION OF τ_o WITH Ccb, n AND Z_o AS PARAMETERS.

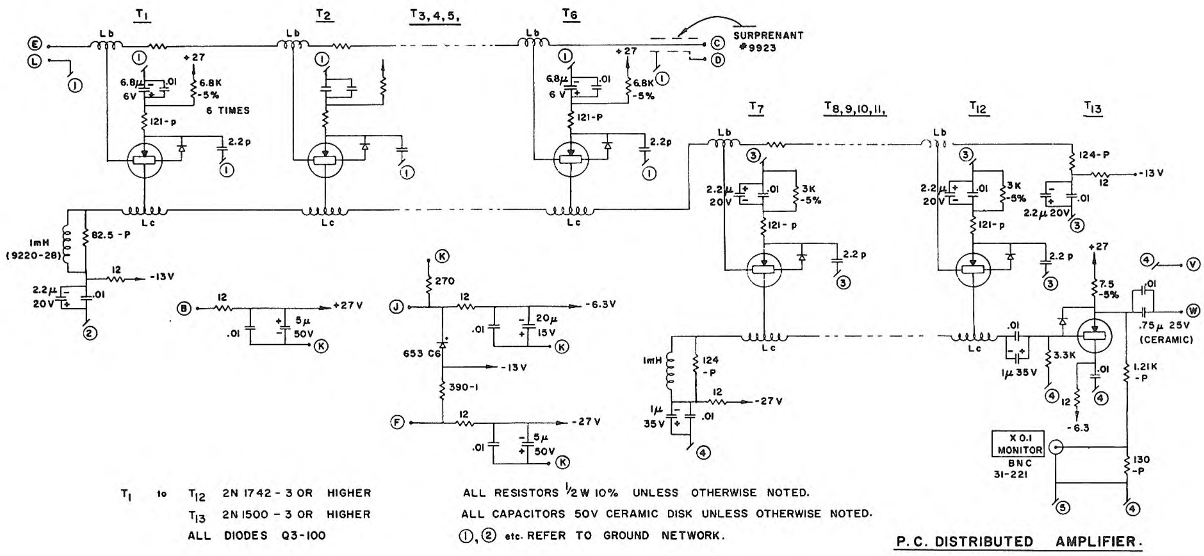


FIG. 6. Schematic of an amplifier for negative pulses with risetime of 2.5 ns and amplification of 10.

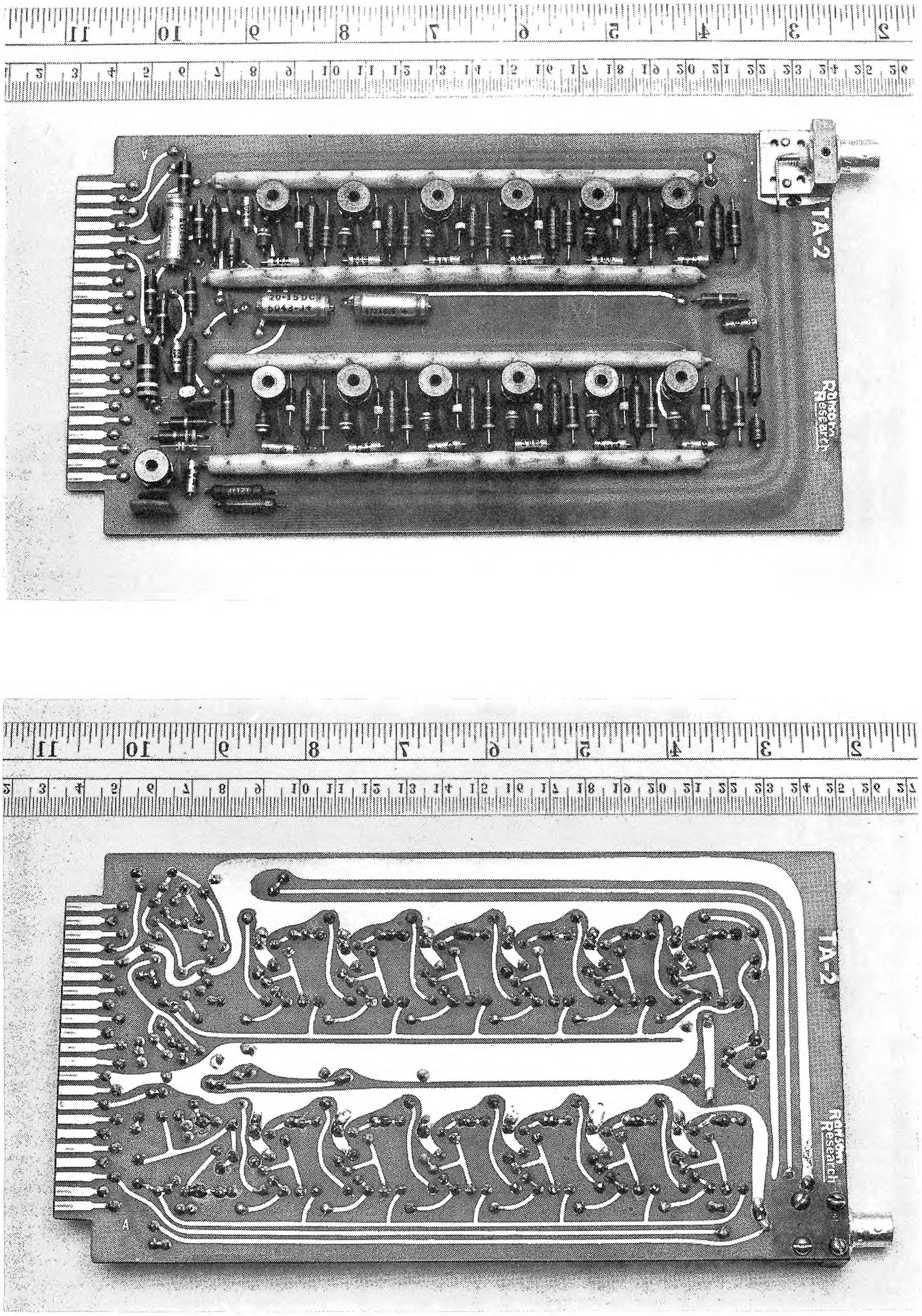
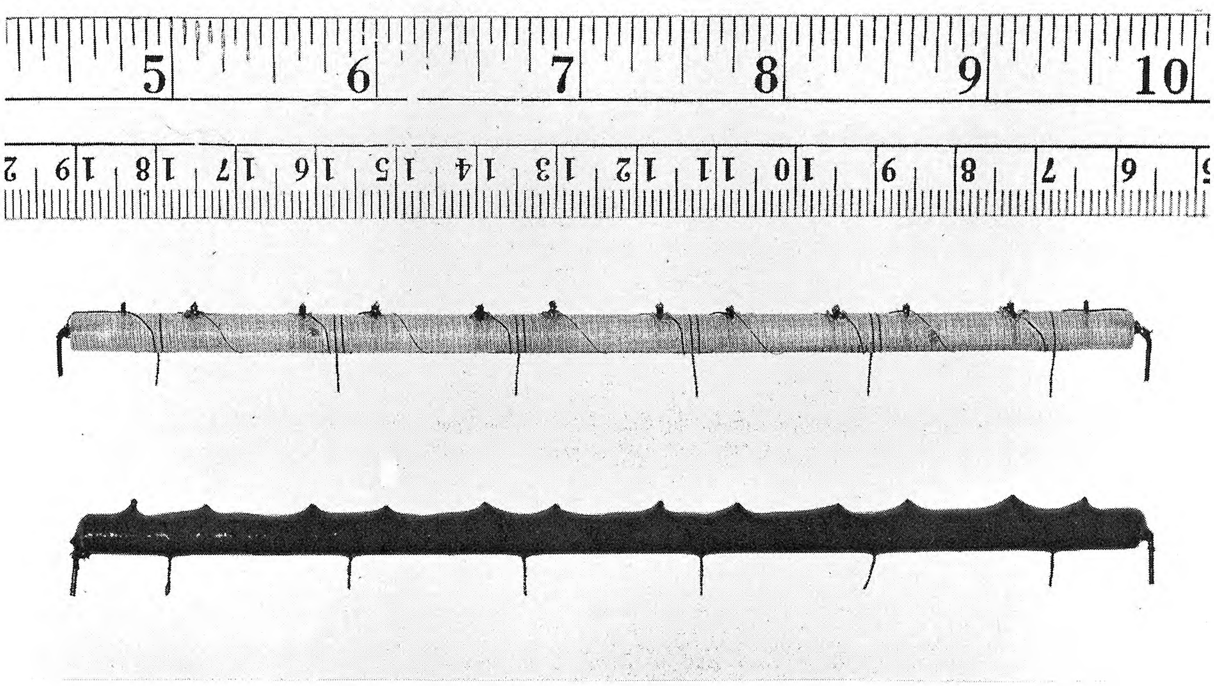


FIG. 7. Photographs of two sides of the amplifier board.



<u>FIG. 8A.</u> Photograph of the base lines before and after encapsulating.

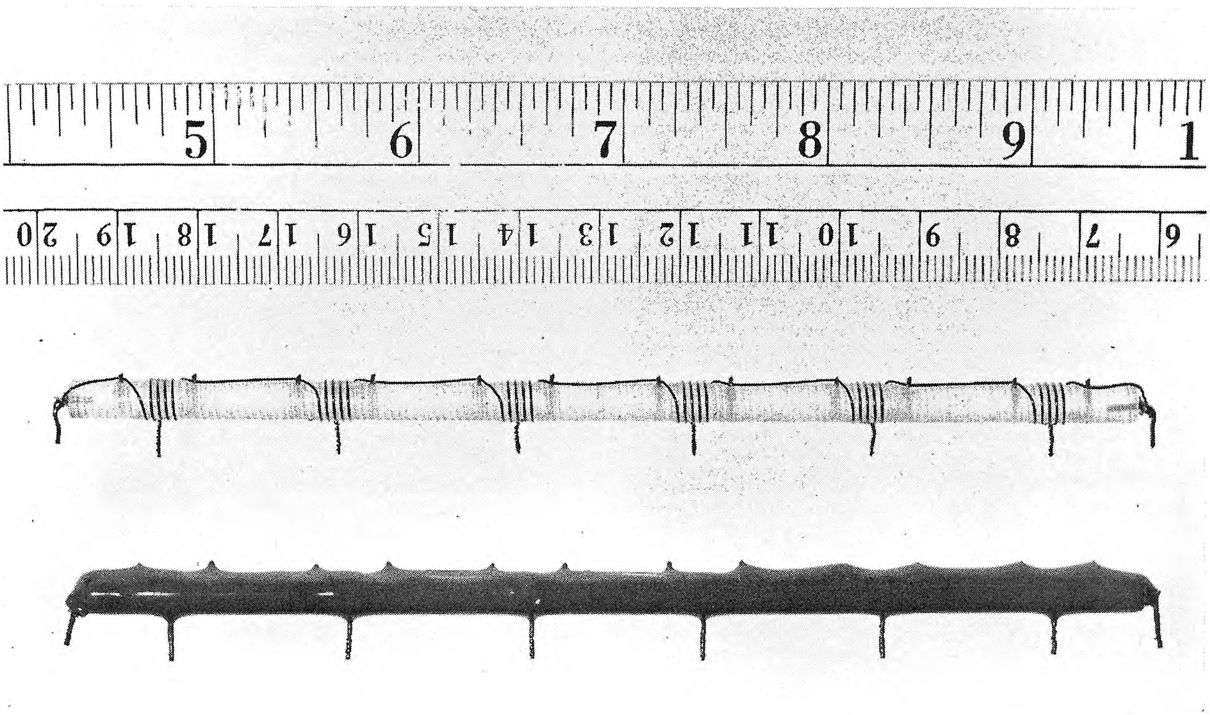


FIG. 8B. Photograph of the collector lines before and after encapsulating.

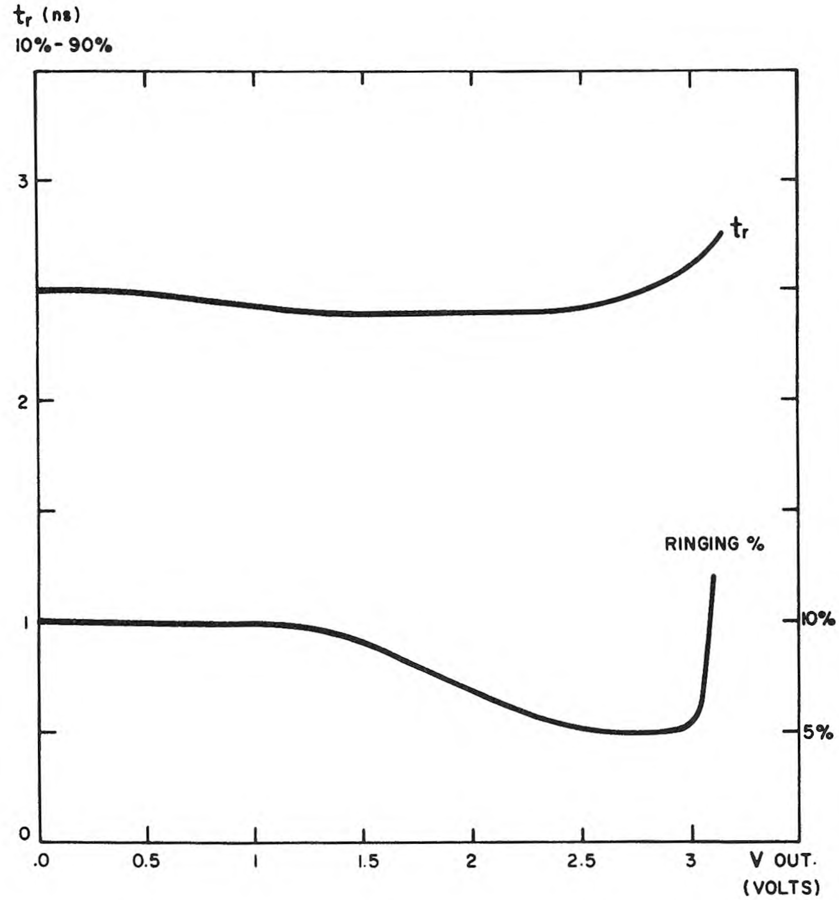


FIG. 9. 10% to 90% RISETIME AND RINGING OF THE AMPLIFIER AS FUNCTION OF THE OUTPUT AMPLITUDE.

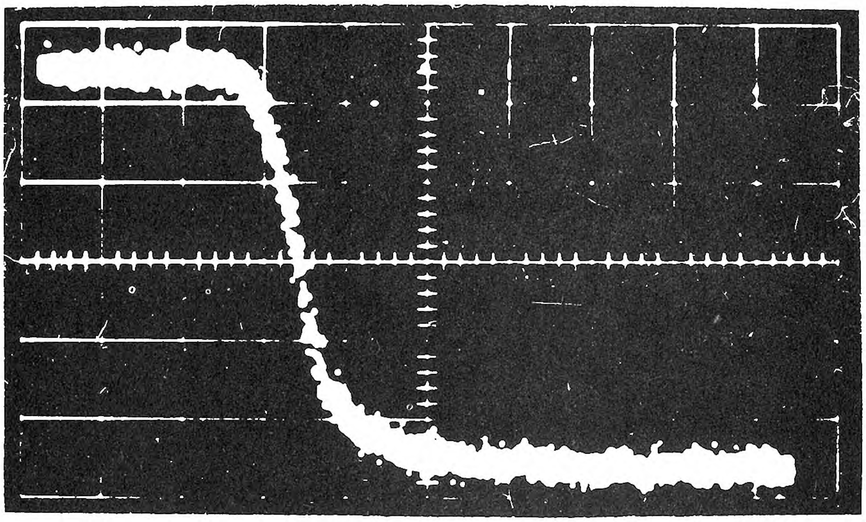


FIG. 10. Step input pulse used for the measurements of Figs. 11 to 13. Sweep speed: 1 ns/major division.

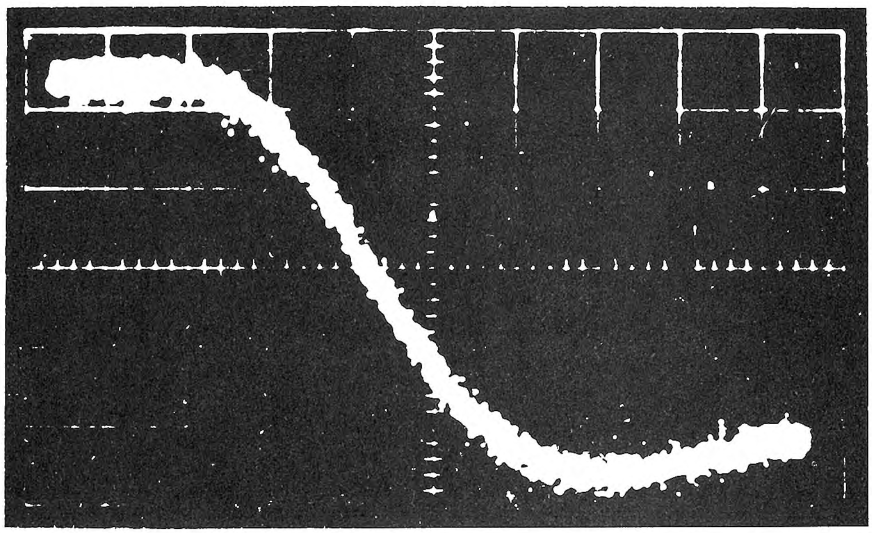


FIG. 11. Output pulse at 2.2 volts output voltage. Sensitivity: 0.44 V/major division. Sweep speed: 1 ns/major division.

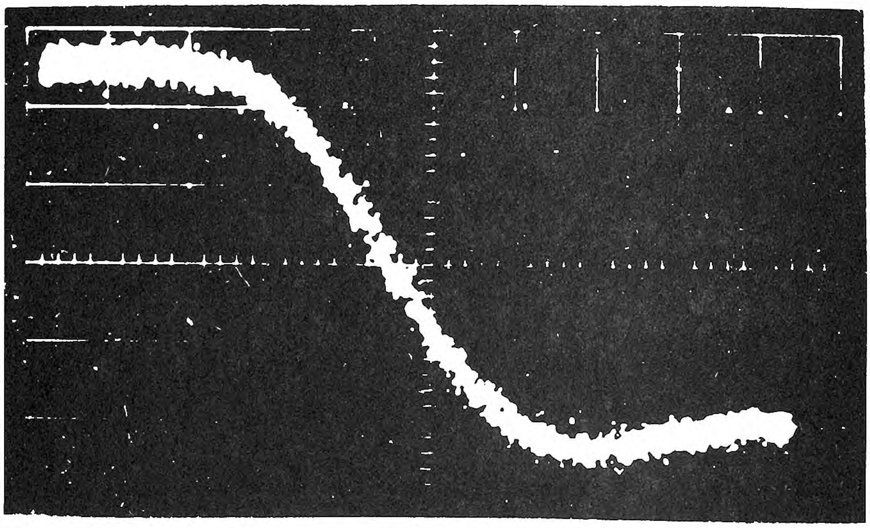


FIG. 12. Output pulse at 0.31 volts output voltage. Sensitivity: 62.5 mV/major division. Sweep speed: 1 ns/major division.

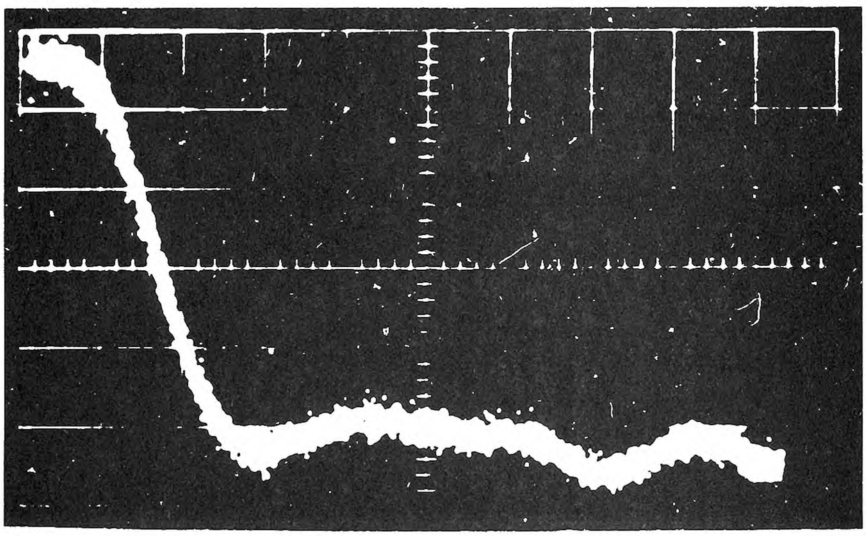


FIG. 13. Output pulse at 0.31 volts output voltage. Sensitivity: 62.5 mV/major division. Sweep speed: 2 ns/major division.

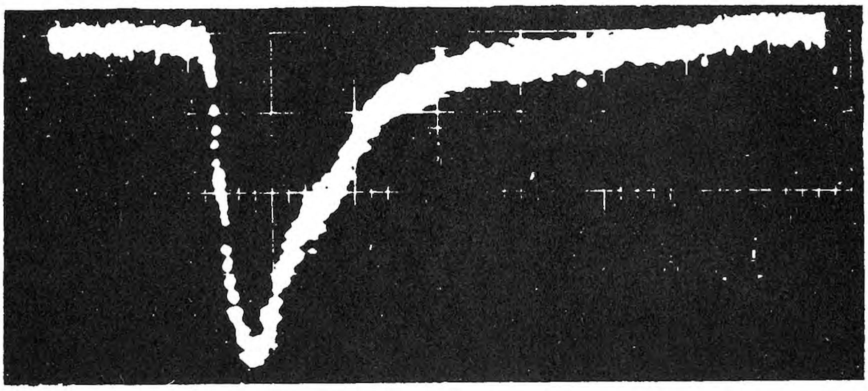


FIG. 14A. Simulated photomultiplier pulse input. Pulse height: 0.35 volts. Sweep speed: 10 ns/major division.

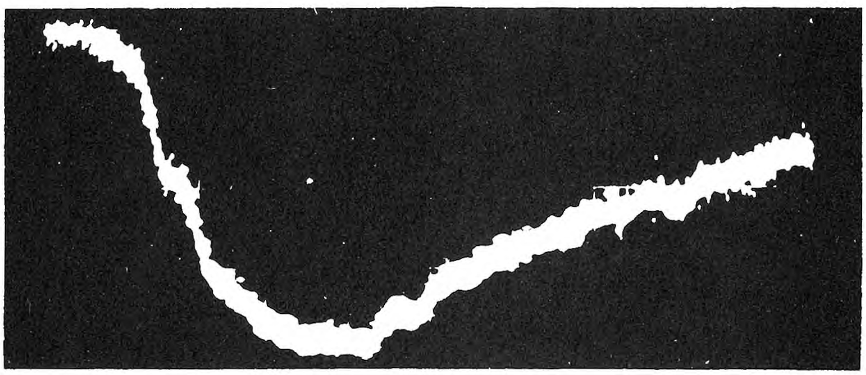


FIG. 14B. Simulated photomultiplier pulse input. Pulse height: 0.35 volts. Sweep speed: 2 ns/major division.

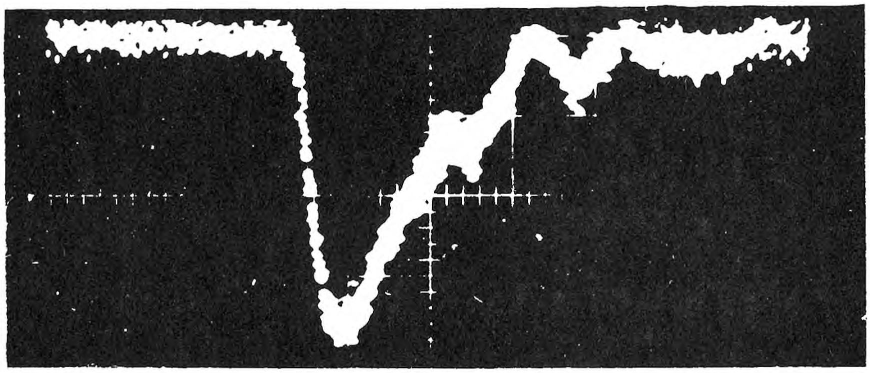


FIG. 15A. Output pulse with input pulse of Fig. 14. Pulse height: 3.15 volts. Sweep speed: 10 ns/major division.

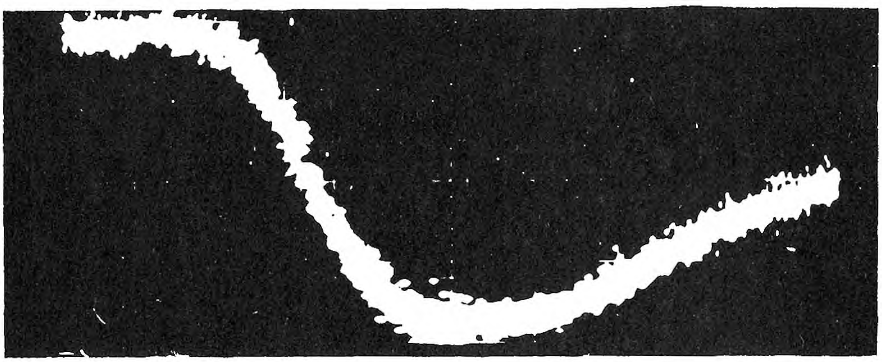


FIG. 15B. Output pulse with input pulse of Fig. 14. Pulse height: 3.15 volts. Sweep speed: 2 ns/major division.